PAN AFRICA CHRISTIAN UNIVERSITY
EXAMININATIONS PAPER

PAN AFRICA CHRISTIAN UNIVERSITY

BACHELORS OF INFORMATION COMMUNICATION TECHNOLOGY

END OF TERM EXAMINATION

DEPARTMENT:	**COMPUTING & INFORMATION TECHNOLOGY**
COURSE CODE:	**BSIT101**
COURSE TITLE:	**DIGITAL ELECTRONICS**
CAMPUS:	**ROYSAMBU**
EXAM DATE:	**FRIDAY**
TIME:	**START HOUR – 11.00AM-1.00PM**

INSTRUCTIONS

- This exam carry a total of SIX Questions of [10 Marks Each]
- Section One (I) is compulsory.
- Answer any 3(Three) Questions from Section Two (II)
- Read all questions carefully before attempting.

SECTION A
(Answer ALL questions in this section)

Question 1 (10 Marks)

a) State two examples of active components in digital electronics. (2 Marks)

b) Discuss two application of Multiplexer. (2 Marks)

c) Explain the use of logic gates in digital circuits. (2 Marks)

d) Define the term base as used in number systems. (2 Marks)

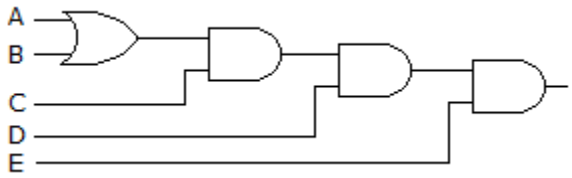
e) Perform the following number conversions $(13A7)_{16}$ to decimal. (2 Marks)

SECTION B

(*(Answer any THREE (3) questions in this section)*

Question Two (10 Marks)

a) Derive the Boolean expression for the logic circuit shown below. (5 Marks)



b) A bulb in a staircase has two switches, one switch being on the ground floor and the other one on the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches, irrespective of the state of the other switch. Discuss the logic of switching of the bulb. (5 Marks)

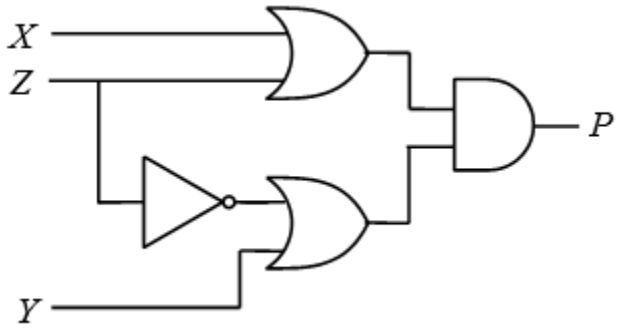
Question Three (10 marks)

a) Using a Karnaugh Map, simplify the following Boolean function into sum of products form

$G(A, B, C, D) = (A + \overline{B} + C).(B + C + \overline{D}).(A + B + \overline{D}).(A + \overline{B} + D).(B + C + D)$

(3 marks)

b) Study the below circuit.Assume that all the logic gates have an equal value of *non-zero* propagation delay and that $X = 0$ and $Y = 0$

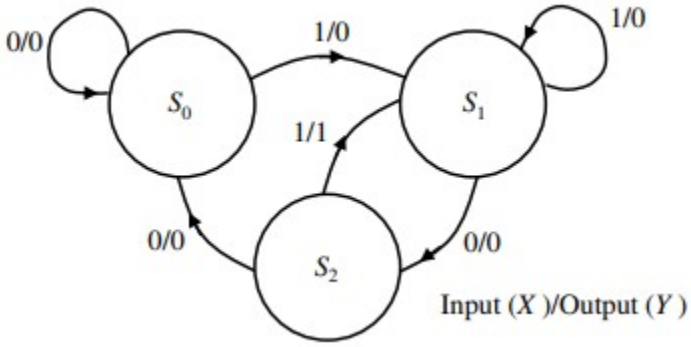


With the aid of a timing diagram, show that a static hazard is present at output *P* when input *Z* changes from 0 to 1. (7 Marks)

Question Four (10 marks)

(a) Show using Boolean algebra (i) X.Y ⊕ X.Y = X.Y + X.Y (2 Marks)

b) Consider the following state machine:



(i) Assuming that the machine starts in state S0 and that the input data sequence at input (X) is appropriately synchronized with the state machine clock, determine the next-state and output sequences for the input sequence 0101011011011. What operation does the machine perform? (7 Marks)

Question Five (10 Marks)

a) Explain briefly the concept of edge triggering in flip-flops. (2 Marks)
b) Write the truth table of XOR gate. (3 marks)
c) Explain the steps involved in the design of asynchronous sequential circuit. (5 marks)

Question Six (10 Marks)

a) a) A finite state machine (FSM) is to be designed such that it counts in the following sequence: $0 \rightarrow 1 \rightarrow 3 \rightarrow 6 \rightarrow 0 \rightarrow 1$ etc.

i) Draw the Moore state diagram for the FSM. (4 Marks)

ii) Distinguish between combinational logic circuits and sequential logic circuits. How are the design requirements of combinational circuits specified. (6 Marks)

